What Is Claimed Is:

1. A method for executing a fail instruction to facilitate transactional execution on a processor, comprising:

transactionally executing a block of instructions within a program;

wherein changes made during the transactional execution are not committed to the architectural state of the processor unless the transactional execution successfully completes; and

if the fail instruction is encountered during the transactional execution, terminating the transactional execution without committing results of the transactional execution to the architectural state of the processor.

2. The method of claim 1, wherein terminating the transactional execution involves discarding changes made during the transactional execution.

3. The method of claim 2, wherein discarding changes made during the transactional execution involves:

discarding register file changes made during the transactional execution;

clearing load marks from cache lines;

draining store buffer entries generated during transactional execution; and

clearing store marks from cache lines.

4. The method of claim 1, wherein terminating the transactional execution additionally involves branching to a location specified by a corresponding start transactional execution (STE) instruction.

5. The method of claim 1, wherein terminating the transactional execution additionally involves branching to a location specified by the fail instruction.

6. The method of claim 1, wherein terminating the transactional execution additionally involves attempting to re-execute the block of instructions.

7. The method of claim 1, wherein if the transactional execution of the block of instructions is successfully completes, the method further comprises:

atomically committing changes made during the transactional execution; and

resuming normal non-transactional execution.

8. The method of claim 1, wherein potentially interfering data accesses from other processes are allowed to proceed during the transactional execution of the block of instructions.

9. The method of claim 1, wherein if an interfering data access from another process is encountered during the transactional execution, the method further comprises:

discarding changes made during the transactional execution; and

attempting to re-execute the block of instructions.

10. The method of claim 1, wherein the block of instructions to be executed transactionally comprises a critical section.

11. The method of claim 1, wherein the fail instruction is a native machine code instruction of the processor.

12. The method of claim 1, wherein the fail instruction is defined in a platform-independent programming language.

13. A computer system that supports a fail instruction to facilitate transactional execution, comprising:

a processor; and

an execution mechanism within the processor;

wherein the execution mechanism is configured to transactionally execute a block of instructions within a program;

wherein changes made during the transactional execution are not committed to the architectural state of the processor unless the transactional execution successfully completes; and

wherein if the fail instruction is encountered during the transactional execution, the execution mechanism is configured to terminate the transactional execution without committing results of the transactional execution to the architectural state of the processor.

14. The computer system of claim 13, wherein while terminating the transactional execution, the execution mechanism is configured to discard changes made during the transactional execution.

15. The computer system of claim 14, wherein while discarding changes made during the transactional execution, the execution mechanism is configured to:

discard register file changes made during the transactional execution;

clear load marks from cache lines;

drain store buffer entries generated during transactional execution; and to

clear store marks from cache lines.

16. The computer system of claim 13, wherein while terminating the transactional execution, the execution mechanism is additionally configured to branch to a location specified by a corresponding start transactional execution (STE) instruction.

17. The computer system of claim 13, wherein while terminating the transactional execution, the execution mechanism is additionally configured to branch to a location specified by the fail instruction.

18. The computer system of claim 13, wherein while terminating the transactional execution, the execution mechanism is additionally configured to attempt to re-execute the block of instructions.

19. The computer system of claim 13, wherein if the transactional execution of the block of instructions is successfully completes, the execution mechanism is configured to:

atomically commit changes made during the transactional execution; and to

resume normal non-transactional execution.

20. The computer system of claim 13, wherein the computer system is configured to allow potentially interfering data accesses from other processes to proceed during the transactional execution of the block of instructions.

21. The computer system of claim 13, wherein if an interfering data access from another process is encountered during the transactional execution, the execution mechanism is configured to:

discard changes made during the transactional execution; and to

attempt to re-execute the block of instructions.

22. The computer system of claim 13, wherein the block of instructions to be executed transactionally comprises a critical section.

23. The computer system of claim 13, wherein the fail instruction is a native machine code instruction of the processor.

24. The computer system of claim 13, wherein the fail instruction is defined in a platform-independent programming language.

25. A computing means that supports that supports a fail instruction to facilitate transactional execution, comprising:

a processing means; and

an execution means within the processing means;

wherein the execution means is configured to transactionally execute a block of instructions within a program;

wherein changes made during the transactional execution are not committed to the architectural state of the processor unless the transactional execution successfully completes; and

wherein if the fail instruction is encountered during the transactional execution, the execution means is configured to terminate the transactional execution without committing results of the transactional execution to the architectural state of the processor.